CLAIMS:

1. An integrated circuit device including a memory array comprising:

at least one sense amplifier having Active, Standby and Sleep modes thereof coupled to complementary bit lines, said sense amplifier having first and second voltage nodes thereof;

a first transistor coupling said first voltage node to a first voltage source, a control terminal of said first transistor being coupled to receive a first control signal; and

a second transistor coupling said second voltage node to a second voltage source, a control terminal of said second transistor being coupled to receive a second control signal.

2. The integrated circuit device of claim 1 wherein said first and second transistors comprise driver/power-gating devices.

3. The integrated circuit device of claim 1 wherein said first and second transistors comprise MOS transistors.

4. The integrated circuit device of claim 3 wherein said first transistor comprises a P-channel device and said second transistor comprises an N-channel device.

5. The integrated circuit device of claim 1 wherein said at least one sense amplifier comprises a latch circuit comprising a pair of cross-coupled inverters.

6. The integrated circuit device of claim 5 wherein said cross-coupled inverters comprise CMOS inverters.

7. The integrated circuit device of claim 1 wherein said first voltage source comprises a supply voltage source and said second voltage source comprises a reference voltage source.

8. The integrated circuit device of claim 7 wherein said supply voltage source comprises VCC and said reference voltage source comprises VSS.

9. The integrated circuit device of claim 1 wherein said first control signal comprises a latch P-channel signal and said second control signal comprises a latch N-channel signal.

10. The integrated circuit device of claim 1 wherein, in an Active Mode of operation, said first control signal is substantially at a level of said second voltage source and said second control signal is substantially at a level of said first voltage source.

11. The integrated circuit device of claim 10 wherein said first control signal is substantially at a reference voltage level and said second control signal is substantially at a supply voltage level.

12. The integrated circuit device of claim 1 wherein, in an Standby Mode of operation, said first control signal is substantially at a level of said first voltage source and said second control signal is substantially at a level of said second voltage source.

13. The integrated circuit device of claim 12 wherein said first control signal is substantially at a supply voltage level and said second control signal is substantially at a reference voltage level.

14. The integrated circuit device of claim 1 wherein, in an Sleep Mode of operation, said first control signal is substantially at a level greater than said first voltage source and said second control signal is substantially at a level lower than said second voltage source.

15. The integrated circuit device of claim 14 wherein said first control signal is substantially at a level greater than said supply voltage level and said second control signal is substantially at a level lower than said reference voltage level.

16. A method for power-gating in an integrated circuit device incorporating a memory having at least one sense amplifier having Active, Standby and Sleep states thereof comprising:

providing first and second transistors for coupling first and second voltage nodes respectively of said sense amplifier to respective first and second voltage sources; and

enabling said first and second transistors in an Active Mode of operation to couple said first and second voltage nodes to said first and second voltage sources respectively.

17. The method of claim 16 further comprising:

disabling said first and second transistors in a Standby Mode of operation to decouple said first and second voltage nodes from said first and second voltage nodes respectively.

18. The method of claim 16 further comprising:

further disabling said first and second transistors in a Sleep Mode of operation by applying a

voltage greater than that of said first voltage source to a control terminal of said first transistor and a voltage lesser than that of said second voltage source to a control terminal of said second transistor.

19. The method of claim 16 wherein said step of enabling said first and second transistors is carried out by applying a voltage substantially equal to a level of said second voltage source to a control terminal of said first transistor and a voltage substantially equal to a level of said first voltage source to a control terminal of said second transistor.

20. The method of claim 17 wherein said step of disabling said first and second transistors is carried out by applying a voltage substantially equal to a level of said first voltage source to a control terminal of said first transistor and a voltage substantially equal to a level of said second voltage source to a control terminal of said second transistor.

21. An integrated circuit device including a memory array comprising:

at least one CMOS sense amplifier coupled to complementary bit lines and including a latch P-channel (LP) and latch N-channel (LN) nodes thereof;

a first transistor coupled between a supply voltage source and said LP node and having a control terminal thereof coupled to receive an LPB signal;

a second transistor coupled between a reference voltage source and said LN node and having a control terminal thereof coupled to receive an LNB signal

wherein said LPB and said LNB signals present Active, Standby and Sleep states thereof.

22. The integrated circuit device of claim 21 wherein said first transistor comprises a P-channel transistor.

23. The integrated circuit device of claim 21 wherein said second transistor comprises an N-channel transistor.

24. The integrated circuit device of claim 21 wherein, in an Active Mode of operation, said LPB signal is substantially at a level of said reference voltage source and said LNB signal is substantially at a level of said supply voltage source.

25. The integrated circuit device of claim 21 wherein, in a Standby Mode of operation, said LPB signal is substantially at a level of said supply voltage source and said LNB signal is substantially at a level of said reference voltage source.

26. The integrated circuit device of claim 21 wherein, in a Sleep Mode of operation, said LPB signal is substantially at a level greater than that of said supply voltage source and said LNB signal is substantially at a level lesser than that of said reference voltage source.

27. A method for power-gating in an integrated circuit device incorporating a memory having a plurality of sense amplifiers comprising:

providing first and second transistors for coupling first and second shared voltage nodes

respectively of said plurality of sense amplifiers to respective first and second voltage sources;

enabling said first and second transistors in an Active Mode of operation to couple said first and second shared voltage nodes to said first and second voltage sources respectively;

disabling said first and second transistors in a Standby Mode of operation to decouple said first and second shared voltage nodes from said first and second voltage nodes respectively; and

further disabling said first and second transistors in a Sleep Mode of operation by applying a voltage greater than that of said first voltage source to a control terminal of said first transistor and a voltage lesser than that of said second voltage source to a control terminal of said second transistor.

28. The method of claim 27 wherein said step of enabling said first and second transistors is carried out by applying a voltage substantially equal to a level of said second voltage source to a control terminal of said first transistor and a voltage substantially equal to a level of said first voltage source to a control terminal of said second transistor.

29. The method of claim 28 wherein said step of disabling said first and second transistors is carried out by applying a voltage substantially equal to a level of said first voltage source to a control terminal of said first transistor and a voltage substantially equal to a level of said second voltage source to a control terminal of said second transistor.

30. An integrated circuit device including a memory array comprising:

a plurality of sense amplifiers coupled to respective complementary bit lines, each of said plurality of sense amplifiers including first and second shared nodes thereof;

a first transistor coupled between a supply voltage source and said first shared node and having a control terminal thereof coupled to receive a first signal;

a second transistor coupled between a reference voltage source and said second shared node and having a control terminal thereof coupled to receive a second signal wherein said first and said second signals present Active, Standby and Sleep states thereof.

31. The integrated circuit device of claim 30 wherein said first transistor comprises a P-channel transistor.

32. The integrated circuit device of claim 30 wherein said second transistor comprises an N-channel transistor.

33. The integrated circuit device of claim 30 wherein, in an Active Mode of operation, said first signal is substantially at a level of said reference voltage source and said second signal is substantially at a level of said supply voltage source.

34. The integrated circuit device of claim 30 wherein, in a Standby Mode of operation, said first signal is substantially at a level of said supply voltage source and said second signal is substantially at a level of said reference voltage source.

35. The integrated circuit device of claim 30 wherein, in a Sleep Mode of operation, said first signal is substantially at a level greater than that of said supply voltage source and said second signal is substantially at a level lesser than that of said reference voltage source.